ISO9001:2000 Certified SCI Quality System

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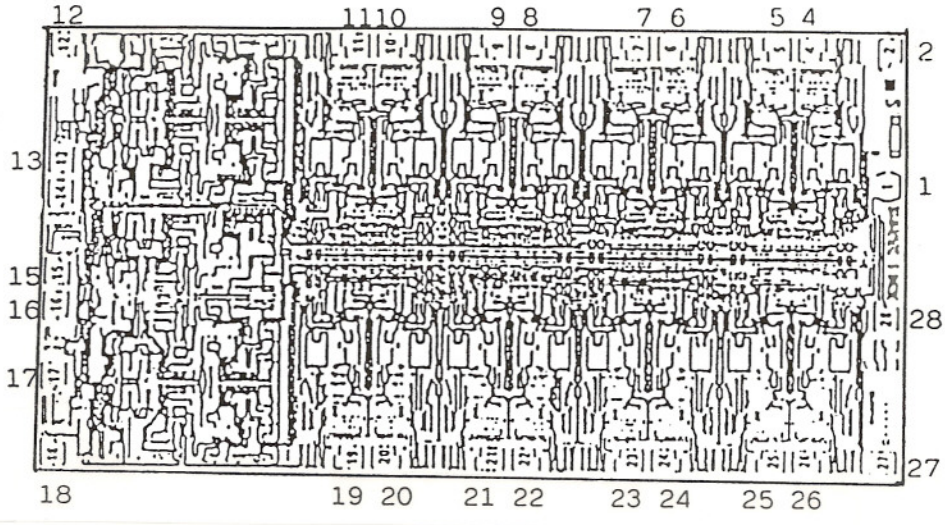
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Pad	Function	Pad	Function	Pad	Function	NOTES:
1	$+V_{SUPPLY}$	11	IN 1B	21	IN 3A	NC = No Connect
2	OUT B	12	GND	22	IN 4A	
3	NC	13	V_{REF}	23	IN 5A	Chip back may
4	IN 8B	14	NC	24	IN 6A	be left floating
5	IN 7B	15	ADDRESS A_2	25	IN 7A	or connected to
6	IN 6B	16	ADDRESS A_1	26	IN 8A	$-V_{SUPPLY}$.
7	IN 5B	17	ADDRESS A_0	27	$-V_{SUPPLY}$	
8	IN 4B	18	ENABLE	28	OUT A	Die layout is
9	IN 3B	19	IN 1A			the same as
10	IN 2B	20	IN 2A			HIO-0507A range.

Topside Metal: Al
Backside: Si
Backside Potential: -V
Mask Ref: 16902
Bond Pads : .004" min

APPROVED BY: CD	**DIE SIZE : .159" x .084"**	**DATE: 2/5/01**
MFG: Harris	**THICKNESS: .019"**	**P/N: HIO-507A-2**